A High Power 2-18 GHz T/R Switch

M.J. Schindler, T.E. Kazior
Raytheon Co., Research Division
131 Spring Street
Lexington, MA 02173

A high power 2-18 GHz T/R switch MMIC has been developed for use in broadband T/R modules. This switch has power handling better than 35 dBm (3.2 watts), 8 dB higher than any previously reported broadband switch. A combination of techniques was used to yield higher power handling while preserving low loss and high isolation. These circuit techniques include: asymmetrical design of the Transmit and Receive arms; the use of dual-gate FETs for handling large voltages, and the use of large FET peripheries for handling large currents.

I. INTRODUCTION

At RF frequencies, power handling in switch FETs is limited by voltage swing in the "off" state (the capacitive state) and current saturation in the "on" state (resistive state)[1]. The present state-of-the-art power handling for broadband (such as 6-18 GHz and dc to 20 GHz) MMIC switches is 24-27 dBm [2][3]. Over narrow frequency bands (10% bandwidth), up to 10 watt power handling has been demonstrated by transforming impedances to reduce current at some FETs and voltage at others [4]. This technique cannot be exploited over a large bandwidth such as 2-18 GHz.

The use of stacked FETs has been reported in a very high power switch operating at lower frequencies (1-2 GHz) [5]. Reactive tuning elements were incorporated to balance the RF voltage distribution across the FETs in the stack. This technique cannot be applied as effectively over a 2-18 GHz band. Nonetheless, the stacked FETs are analogous to the dual-gate FETs used in this work. Note that the use of dual-gate FETs in place of a stack of individual FETs reduces device area with a resulting reduction in parasitic series inductance through the FET and shunt capacitance from the FET to ground. These parasitics must be minimized in order to ensure low insertion loss to 18 GHz. Power handling is somewhat lower for the dual-gate FET than for the stacked FETs, since RF voltage cannot be distributed as uniformly across the gates. Off-state capacitance is higher for a dual-gate FET than a stacked FET, since the close proximity of the elements leads to additional parasitic capacitances.

II. DESIGN APPROACH

Conventional broadband 1 x 2 switches use a combination of series and shunt switch FET, and provide 27 dBm of power handling. Insertion loss is typically less than 2 dB, and isolation is at least 30 dB [3]. In the design of the 2-18 GHz high power T/R switch presented in this paper, the same basic circuit approach used in conventional lower power switches was used, but three techniques were employed to increase power handling.

The first of the techniques used to increase power handling is the replacement of conventional single switch FETs with dual-gate FETs in some circuit locations. In a simplistic analysis, a dual-gate FET can be thought of as two single-gate FETs in series. The RF voltage swing can be distributed across these two devices, extending power limits imposed by voltage limiting. In reality, there is significant capacitive coupling between the two FETs within a dual-gate FET. This cross coupling decreases power handling slightly on the order of 1 dB.

Compared to the single-gate FETs used in conventional series and shunt FET broadband switches, the on state resistance (R_{on}) of a dual-gate FET is considerably higher. In order to maintain a reasonably low insertion loss, it is necessary to increase the periphery of these devices considerably. As is explained below, the periphery of a dual-gate FET can be considerably larger than the periphery of a single-gate FET.

The second of the techniques used to increase power handling is to increase the periphery of some FETs. Large peripheries are used to provide higher RF current handling. A major problem with increasing peripheries is the resulting increase in the off state capacitance (C_{off}). High values of C_{off} cannot be accommodated by the switch circuit without resulting in much higher insertion loss. In order to incorporate large peripheries without increasing insertion loss dual-gate FETs are used, since their C_{off} in considerably lower than that of a single-gate FET.

The third technique employed to increase power handling is the use of an asymmetrical switch design; that is to say, the circuit is designed so that the Transmit and Receive arms are different. For example, the shunt FETs in the Transmit arm and the series FET in the Receive arm must handle the largest RF voltage swings, and therefore use dual-gates. The series FET in the Transmit arm and the shunt FETs in the Receive arm must handle the largest RF currents, therefore have large peripheries. In some cases, dual-gate FETs are used in these locations as well simply to reduce C_{off}.

The schematic of the 2-18 GHz high power switch is shown in Figure 1. The periphery of each device is indicated. The switch is designed to handle highest power in the Transmit mode. Note that FET2, FET3, and FET4 must all handle large voltage swings, and therefore dual-gates are used. The peripheries of these devices are also quite large in order to reduce "on" resistance. FET1 and to a lesser extent FET5 must handle

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large currents, therefore periphery must be large. These devices use dual-gates to reduce "off" capacitance. FET6 is the only device not using dual-gates.

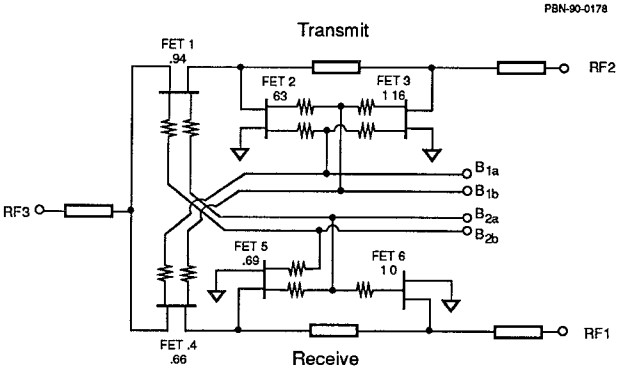


Figure 1. Schematic of the 2-18 GHz high power T/R switch.

The equivalent circuit of the switch in Transmit mode is shown in Figure 2a. The periphery of each device is indicated next to its equivalent circuit element(s). Dual-gate FETs are indicated by a "DG", single FETs by an "SG." A simplified switch equivalent circuit is shown in Figure 2b. In this case, the receive arm is approximated as a resistance. Loss mechanisms are most apparent in the simplified equivalent circuit.

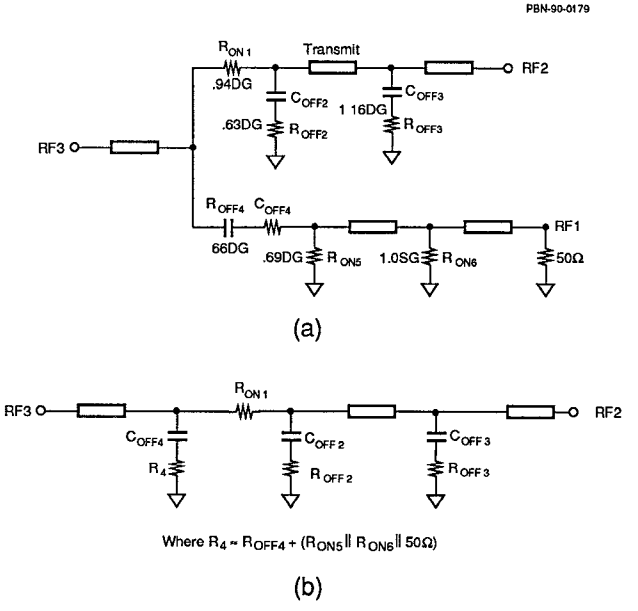


Figure 2. (a) Complete equivalent circuit of the switch in Transmit mode, (b) simplified equivalent circuit.

There are two primary contributors to insertion loss. The first is the on resistance of the series FET, in this case, R_{on1}. The second contributor is loss through the shunt RC elements, similar to gate line loss in a distributed amplifier [6]. The periphery of FET1 is quite large, .94 mm, ensuring low insertion loss despite the fact that it is a dual-gate device. The shunt elements are all dual-gate FETs. Since this reduces C_{off}, this also minimizes insertion loss.

The equivalent circuit of the switch in Receive mode is shown in Figure 3. This figure uses the same format as /figure 2. Note that the series FET in Receive (FET4) has a smaller periphery than the series FET in the Transmit mode (FET1). The resulting difference in R_{on} causes insertion loss to be higher in the Receive mode. The shunt elements are lossier in the Receive mode as well. Shunt capacitance C_{off1} in Receive is higher than C_{off4} in Transmit because of larger FET periphery. C_{off6} in Receive is higher than C_{off3} in Transmit because FET6 is a single-gate device and FET3 is a dual-gate device. Thus the insertion loss in the Receive mode is expected to be higher than the insertion loss in the Transmit mode.

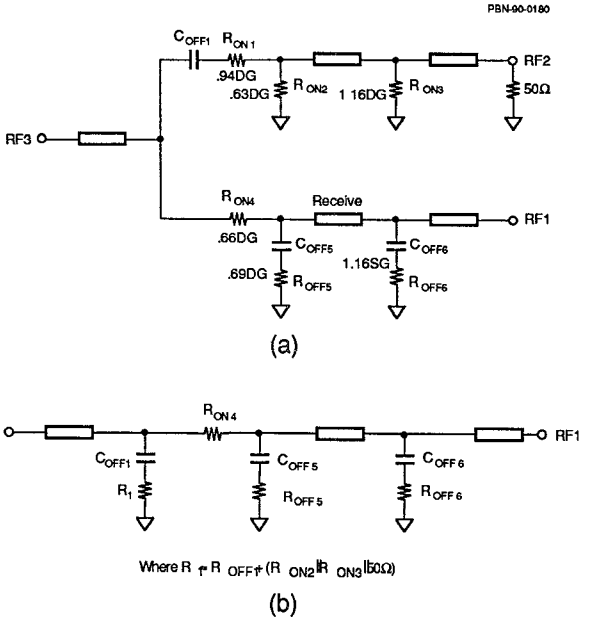


Figure 3. (a) Complete equivalent circuit of the switch in Receive mode, (b) simplified equivalent circuit.

The higher loss in the Receive mode is the result of a deliberate design trade-off. The size of the series FETs plays a large role in insertion loss. By increasing the periphery of the series FET in the Transmit mode large (FET1), R_{on} is reduced which provides a low Transmit insertion loss; C_{off} is simultaneously increased, which provides a high insertion loss in Receive. Similarly, reducing the periphery of the series FET in Receive mode increases insertion loss in Receive, but decreases insertion loss in Transmit. In the design of the 2-18 GHz T/R switch presented in this paper, the insertion loss in Transmit was paramount, and was reduced at the cost of Receive insertion loss.

IV. MMIC Implementation

The finished MMIC is quite small, 0.9 mm x 1.5 mm, or 035" x .060" as can be seen in Figure 4. The FETs all have a 0.5 µm gate length. The nominal source-drain space is 3.5 µm for single-gate FETs, 7.5 µm for dual-gate FETs. The dual-gate FET gate pitch is 4 µm. VPE material was used with a channel doping of 2 x 10^{17} cm^{-3}, and an n^+ doping of 4 x 10^{18} cm^{-3}. These circuits were passivated with 2000 Å of silicon nitride. There are no capacitors in this circuit. The wafer

was thinned to 100 μm, and 20 x 100 μm via holes were dry etched.

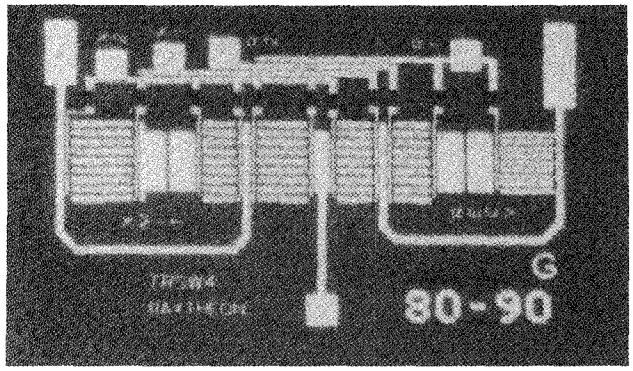
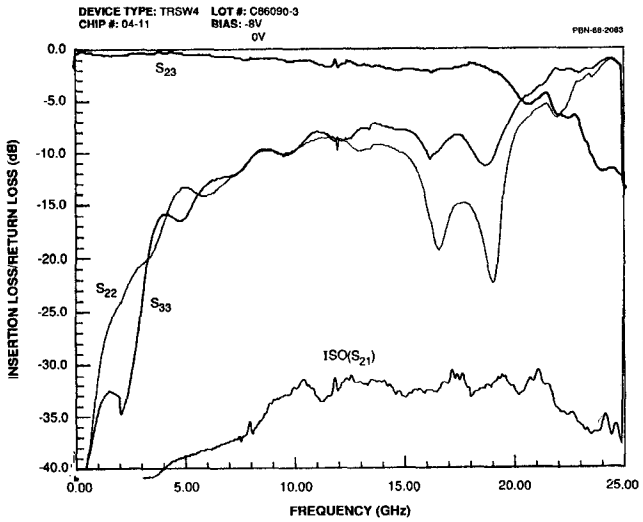


Figure 4. Photograph of the 2-18 GHz high power switch.

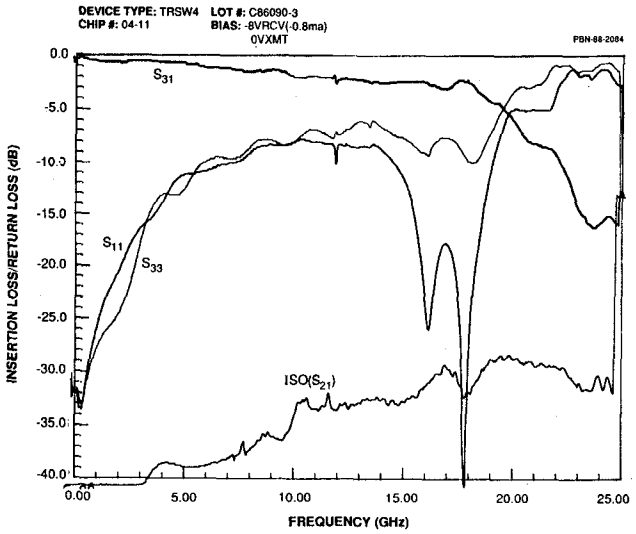
Gate bias is provided through resistors comprised of multiple open gate FETs in series, each 10 μm wide, for a total resistance of approximately 2 kΩ per resistor. Separate gate connections are made for each gate in the dual-gate FETs, and independent bias connections were provided. In actual circuit use, both gates of each dual-gate FET were biased to the same potential, so only two complementary bias controls were required. No off chip bias circuitry was used.

V. Results

The measured small signal performance is shown in Figure 5. Figure 5a shows performance for the transmit state; Figure 5b shows performance for the receive state. In Transmit mode the insertion loss is 2 dB, or less, from dc to 18 GHz. In Receive mode, the insertion loss is 2.5 dB, or less, from dc to 18 GHz. Isolation is better than 30 dB in both cases. Return losses are generally better than 10 dB to 18 GHz, but reach 8 dB at some points.



(a)



(b)

Figure 5. Small signal performance of the T/R switch (a) in Transmit mode and (b) in Receive mode.

The power handling of the switch in Transmit mode is shown in the transfer curves in Figure 6. Curves are given for a number of frequencies over the band. Incident power levels up to 35-36 dBm (3.2-4 watts) are handled without significant change in insertion loss. A gate bias voltage of -14 volts is applied which, with a bias of -10 volts power handling, drops to 32 dBm, and with a bias of -7 volts power handling, drops to 29 dBm.

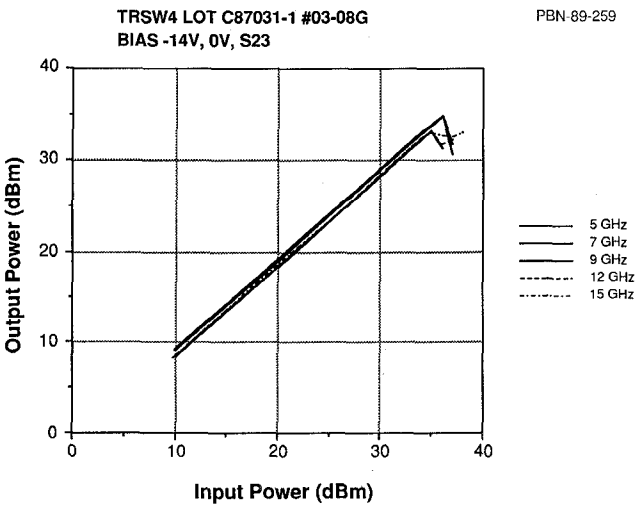


Figure 6. Power transfer curves for the T/R switch in Transmit mode; output vs. input power is shown.

Power handling in the Receive mode is shown in the transfer curves in Figure 7. Incident power levels up to 32-33 dBm (1.6-2 watts) are handled without significant degradation in insertion loss. A -14 volt bias is used for this measurement as well.

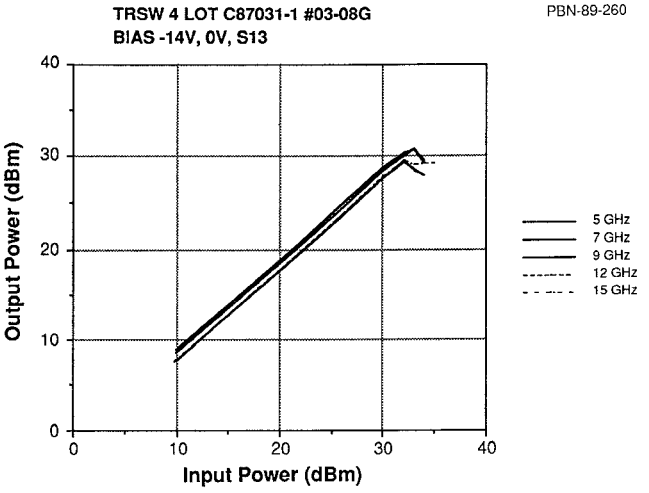


Figure 7. Power transfer curves for the T/R switch in Receive mode; output vs. input power is shown.

IV. Summary

A combination of approaches was used to increase the power handling of a broadband series and shunt FET switch. Power handling is 35-36 dBm, more than 8 dB higher than for a conventional circuit. Other switch performance attributes were maintained, excepting a small increase in insertion loss in the Receive mode, which is about 0.5 dB higher than for a conventional design.

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References

[1] Y. Ayasli, "Microwave Switching with GaAs FETs," Microwave Journal, vol. 25, no. 11, 1982, pp. 61-74.

[2] Y. Ayasli, R. Mozzi, L. Reynolds, T.Tsukii, "6-19 GHz GaAs FET Transmit Receive Switch," 1983 GaAs IC Symposium Digest, pp. 106-108.

[3] M. Schindler, M. Miller, K. Simon, "DC-20 GHZ NxM Passive Switches," IEEE T-MTT, vol. 36, no. 12, Dec. 1988, pp. 1604-1613.

[4] Y. Ayasli, R. Mozzi, L. Hanes, L. Reynolds, "An X-Band 10 W Monolithic Transmit-Receive GaAs FET Switch," IEEE Monolithic and Millimeter-wave Monolithic Symposium Digest, 1982, pp. 42-46.

[5] M. Shifrin, P. Katzin, Y. Ayasli, "High Power Control Components Using a New Monolithic FET Structure," IEEE Monolithic and Millimeter-wave Monolithic Symposium Digest, 1989, pp. 51-56.

[6] M. Schindler, A. Morris, "DC-40 GHZ and 20-40 GHZ MMIC SPDT Switches," IEEE T-MTT, vol. 35, no. 12, Dec. 1987, pp. 1486-1493.